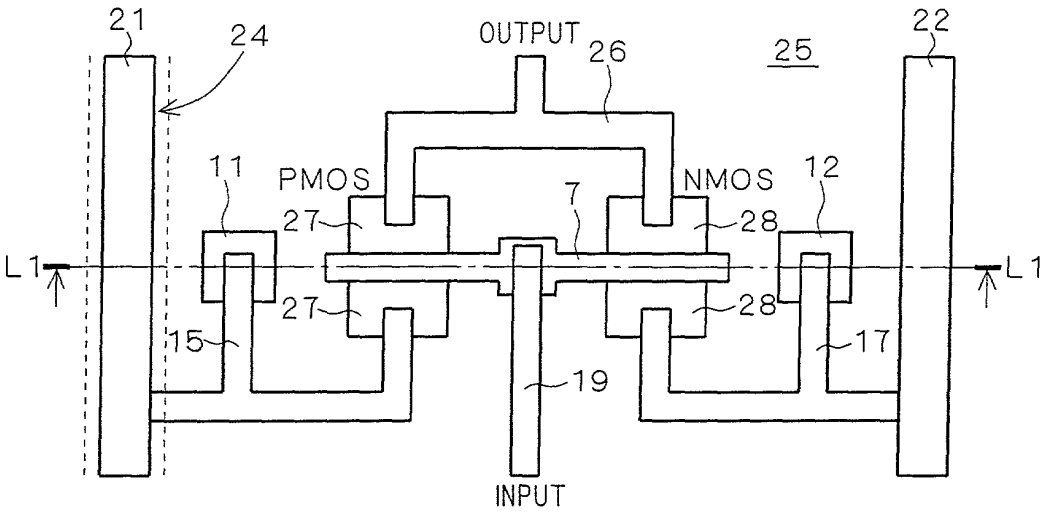
FIG. 1


21
24
OUTPUT
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PMOS
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NMOS
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27
28
L1
L1
27
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17
19
INPUT

FIG. 2

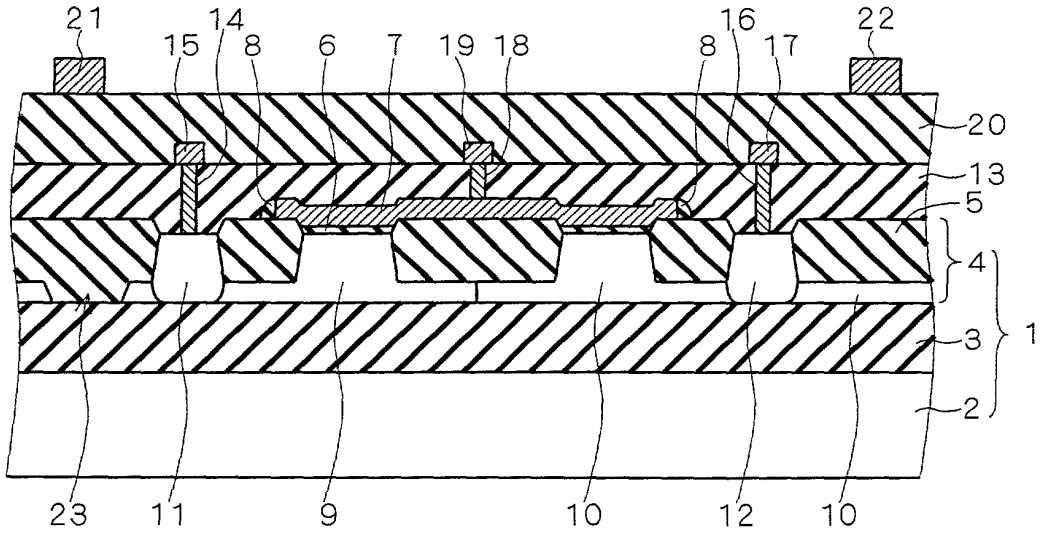
21
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FIG. 3

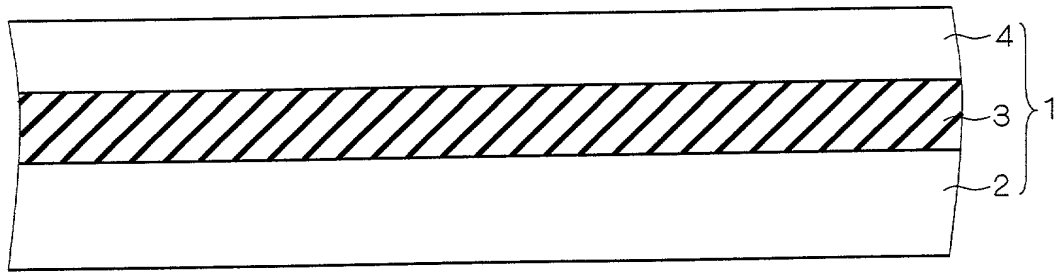

FIG. 4

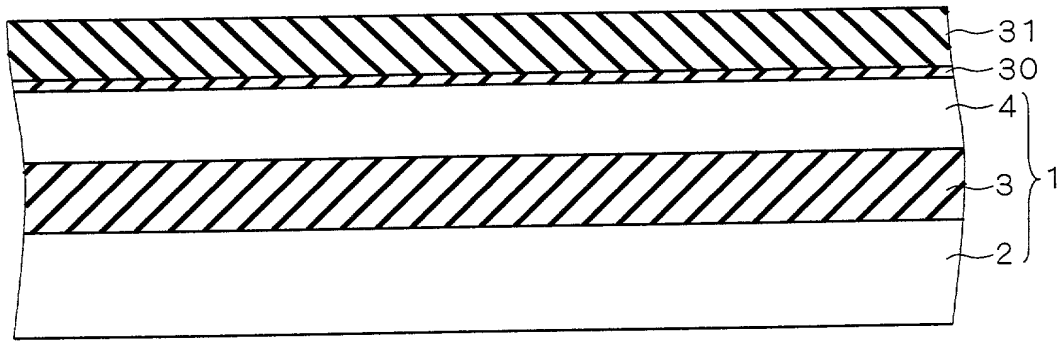

FIG. 5

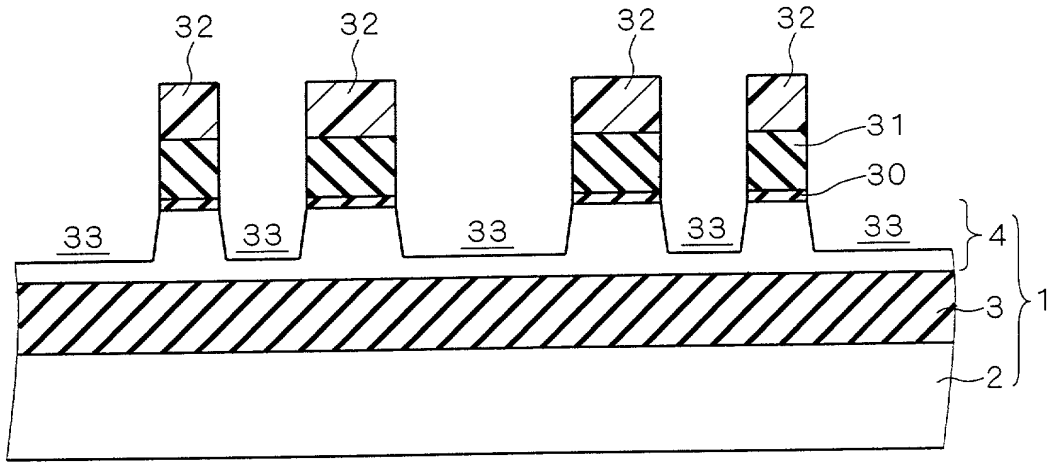

FIG. 6

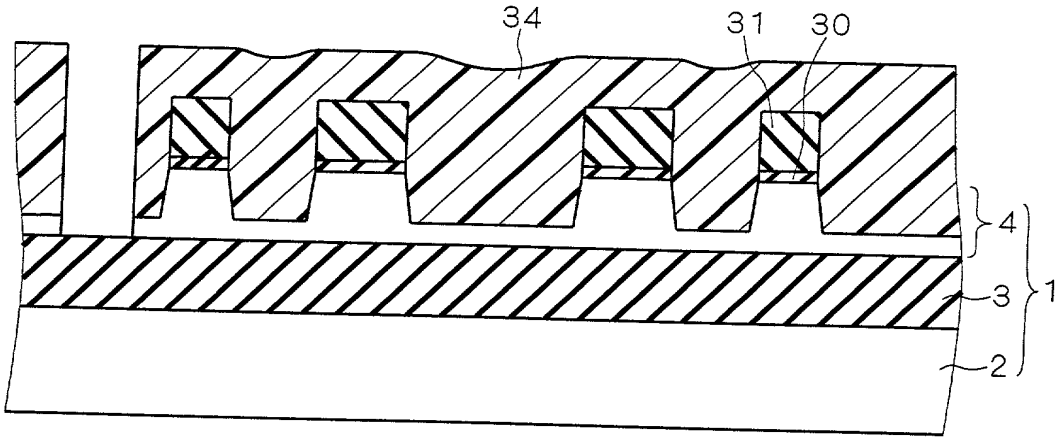

FIG. 7

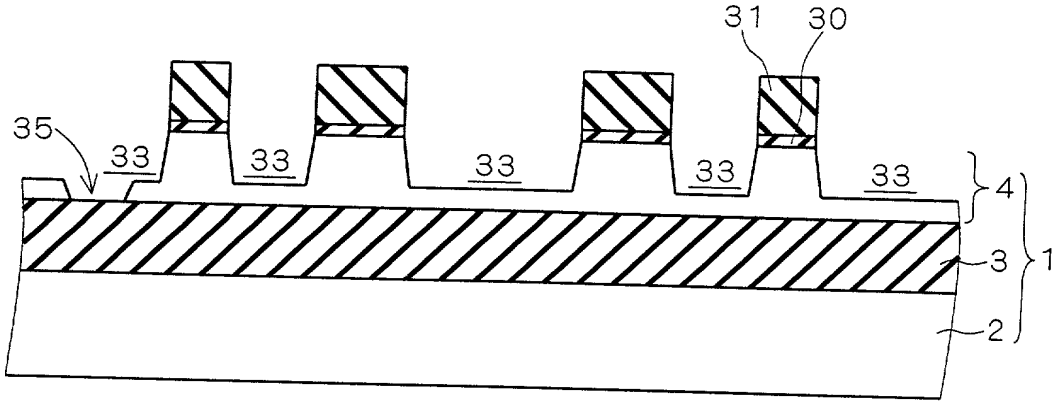

FIG. 8

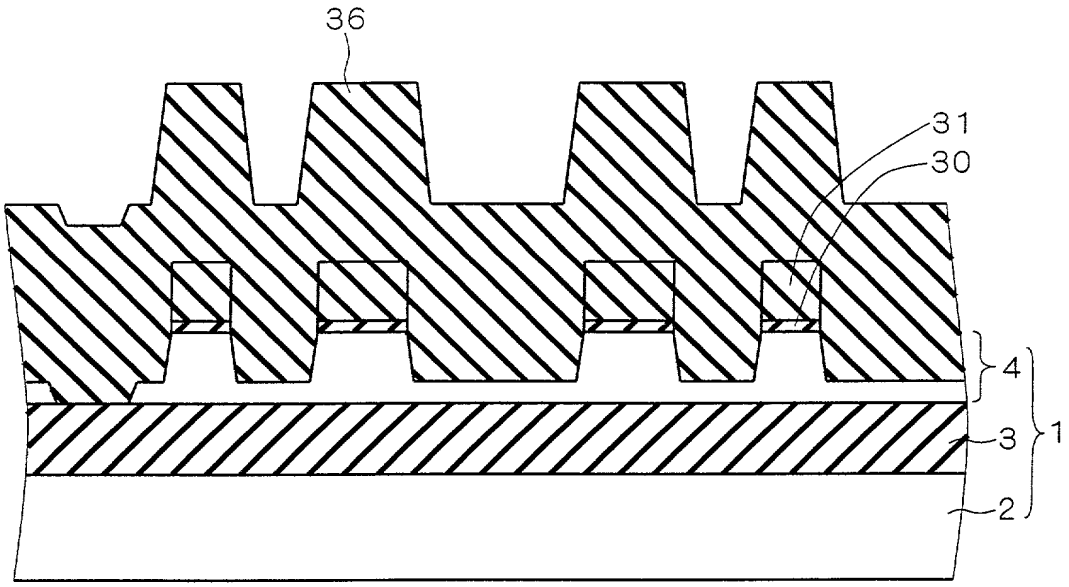

FIG. 9

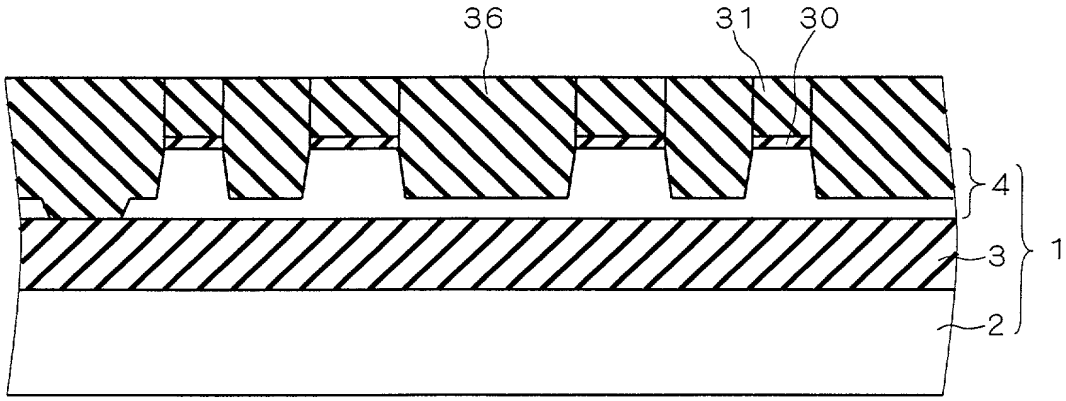

FIG. 10

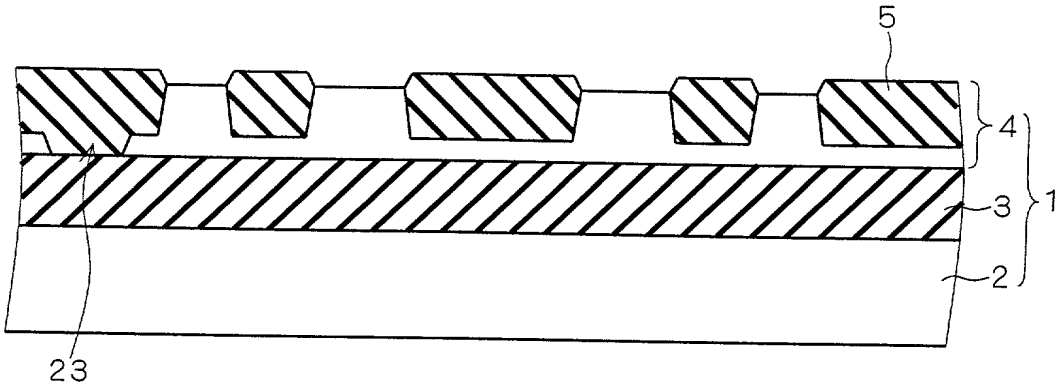

FIG. 11

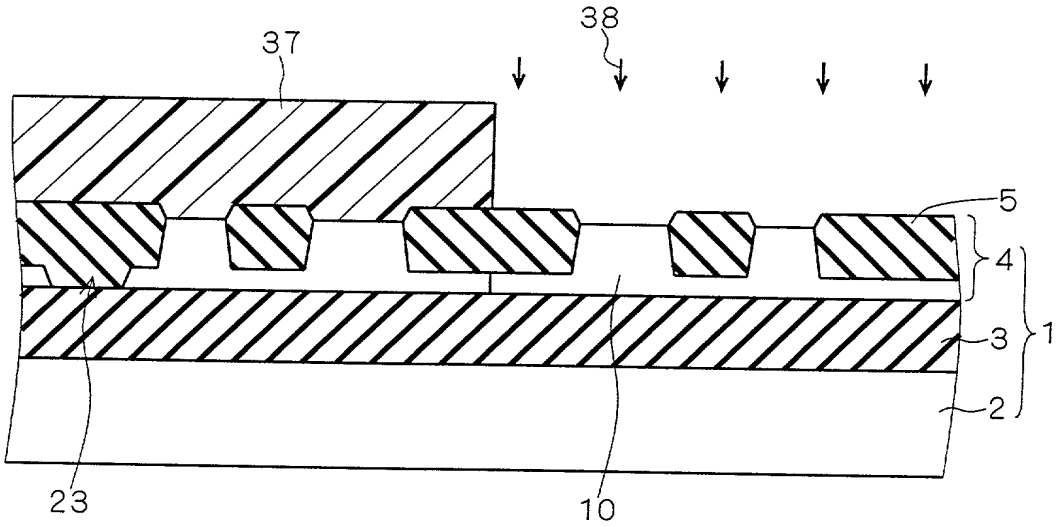

FIG. 12

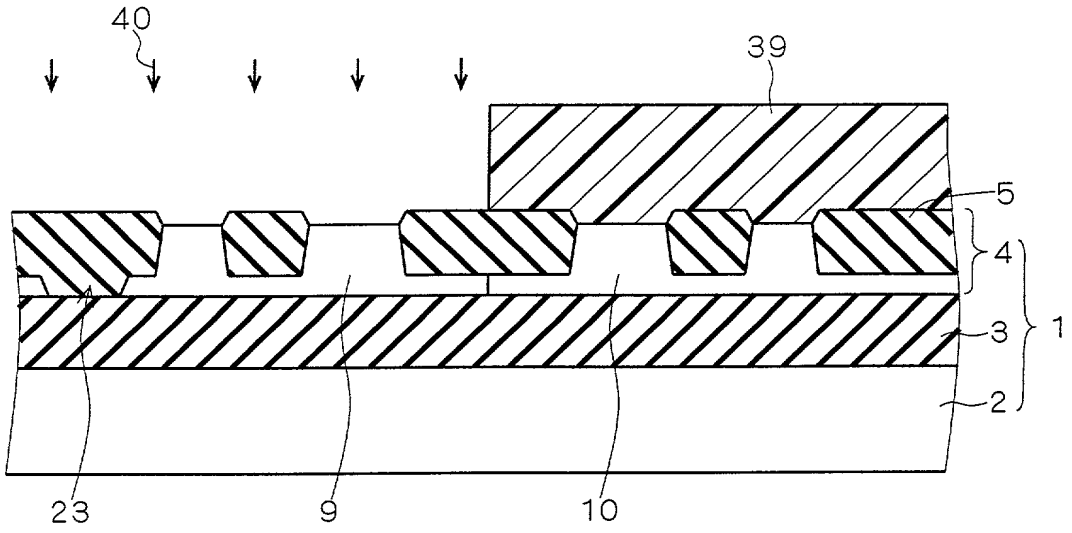

FIG. 13

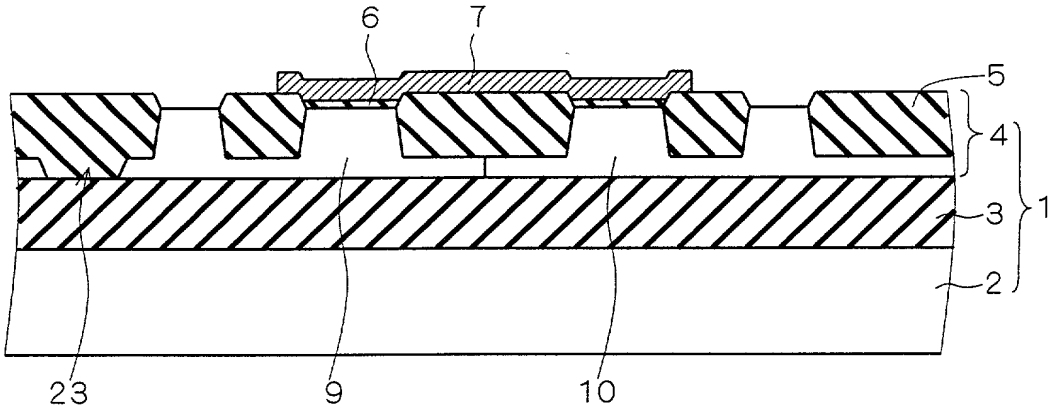

FIG. 14

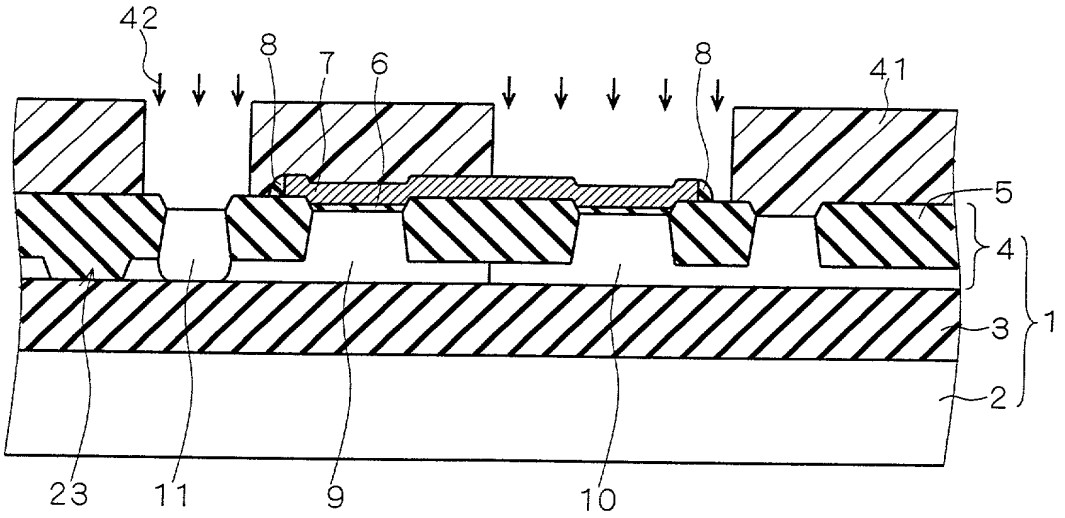

FIG. 15

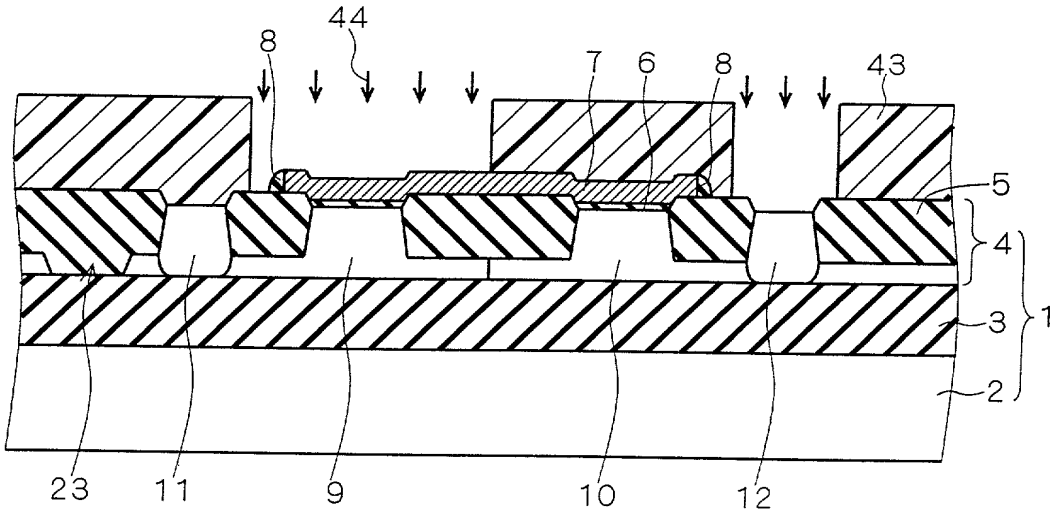

FIG. 16

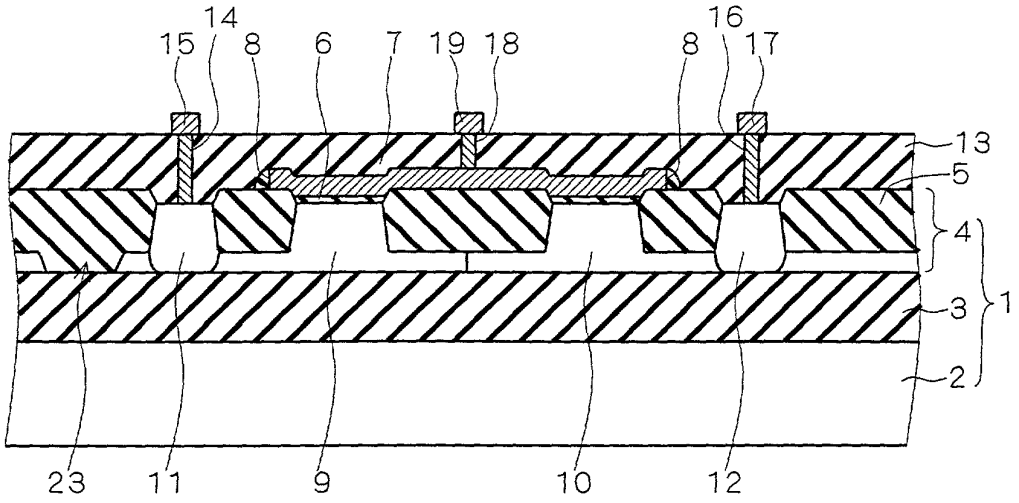
14
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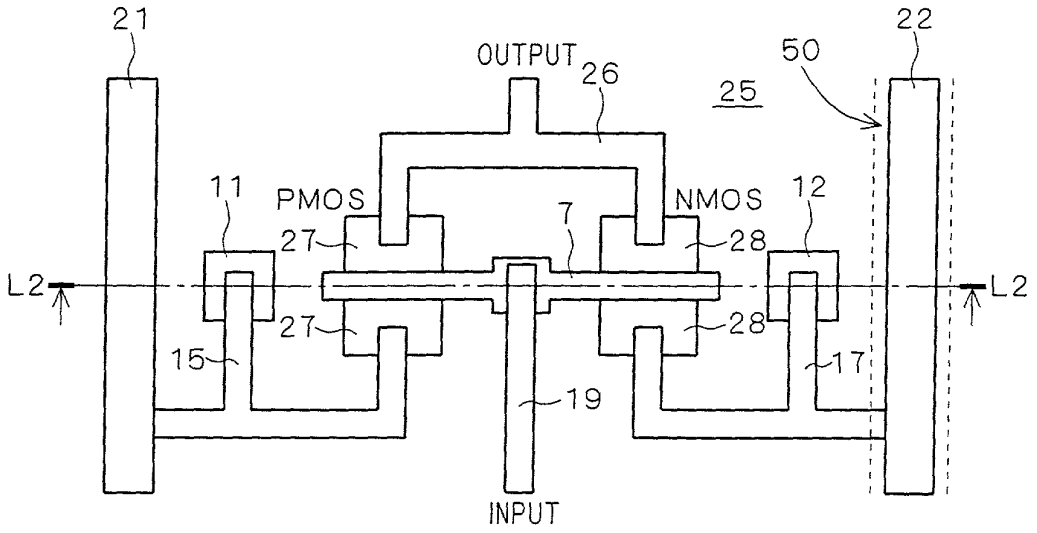
FIG. 17


21
OUTPUT
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50
22
11
PMOS
NMOS
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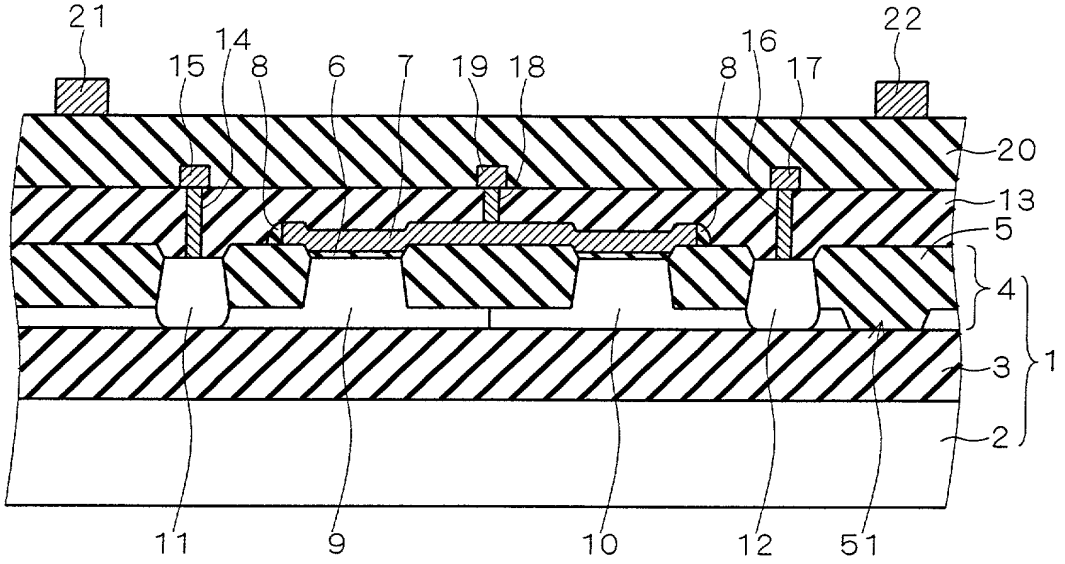
27
28
L2
L2
27
28
15
17
19
INPUT

FIG. 18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6
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16
17
22
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13
5
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1
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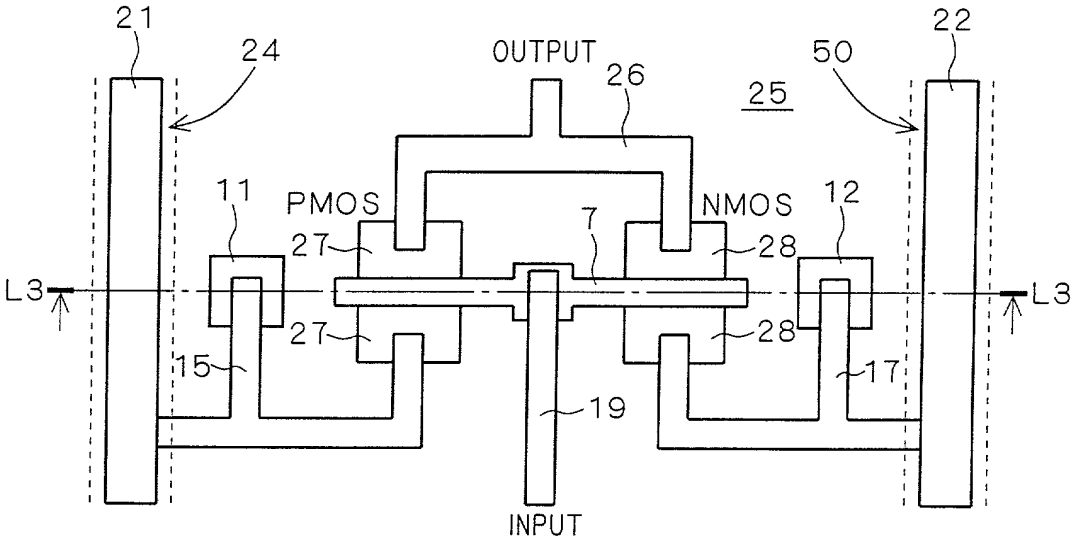
11
9
10
12
51

FIG. 19


21
24
OUTPUT
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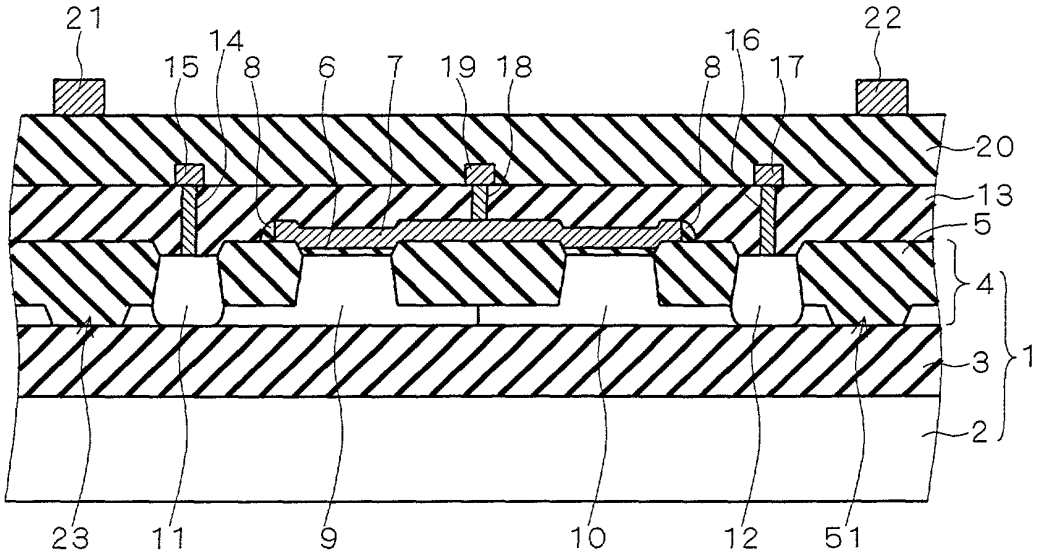
25
50
22
11
PMOS
7
NMOS
12
27
28
L3
L3
27
28
15
17
19
INPUT

FIG. 20


21
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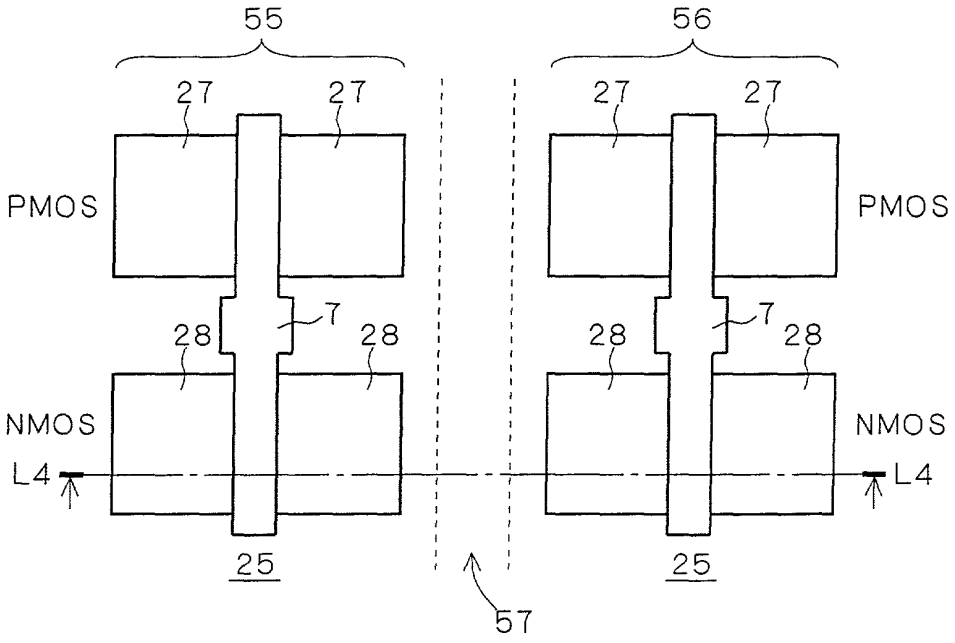
12
51

FIG. 21


55
56
27
27
27
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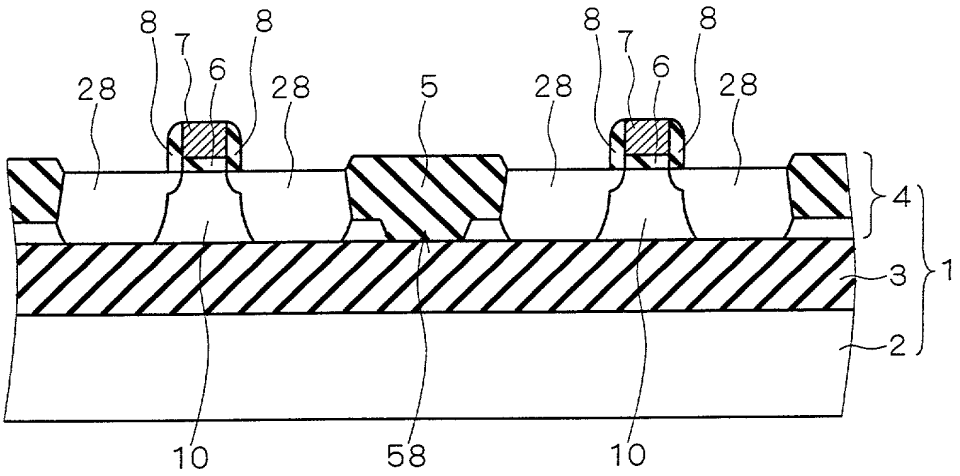
PMOS
PMOS
28
7
28
28
7
28
NMOS
NMOS
L4
L4
25
25
57

FIG. 22


8
7
6
8
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5
28
8
7
6
8
28
4
3
1
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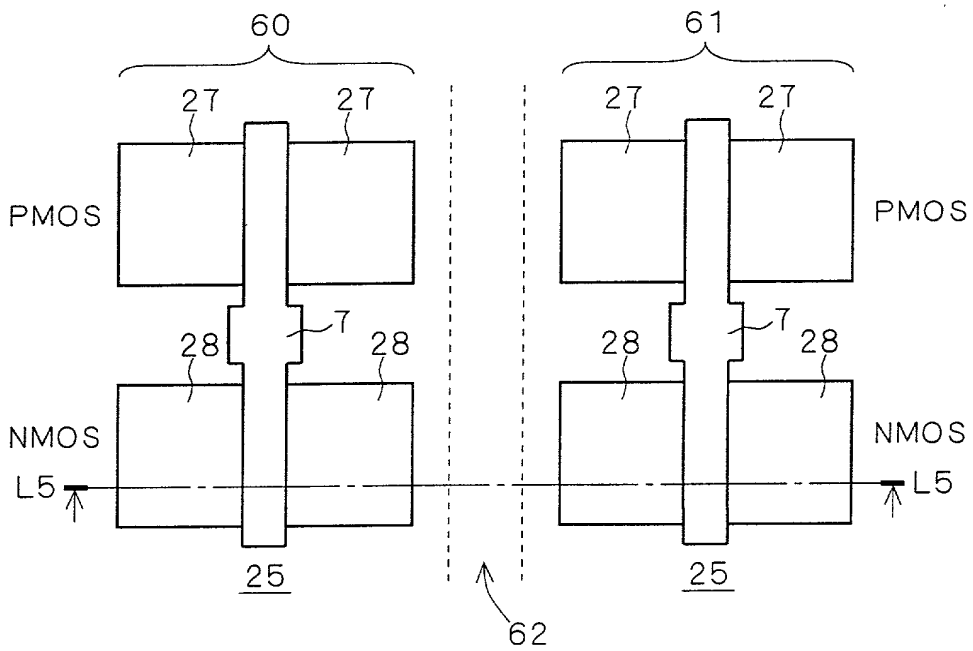
10
58
10

FIG. 23


60
61
27
27
27
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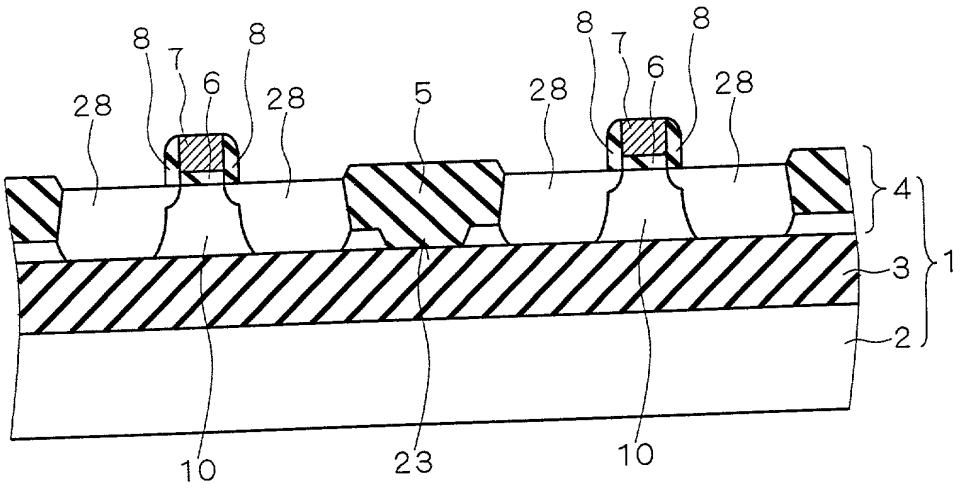
PMOS
PMOS
7
7
28
28
28
28
NMOS
NMOS
L5
L5
25
25
62

FIG. 24


8
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4
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FIG. 25

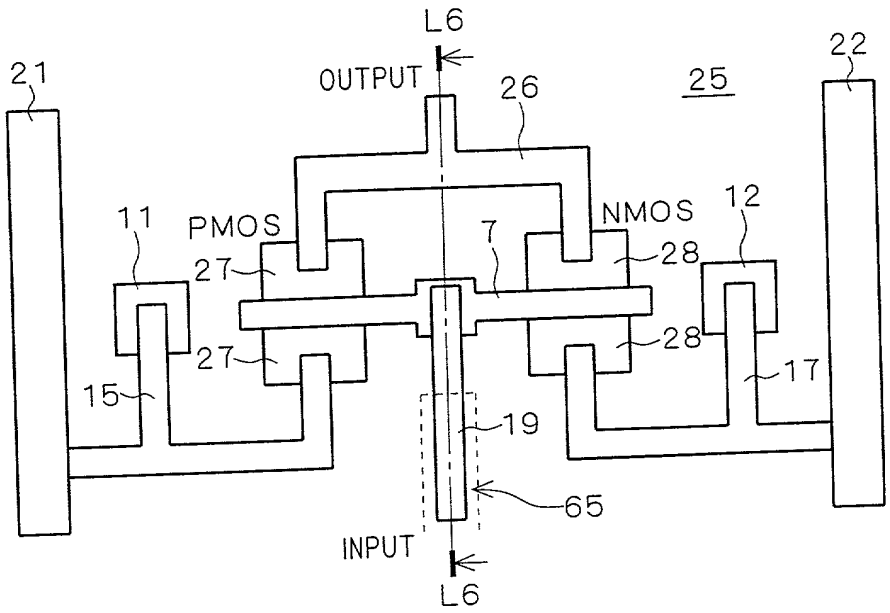

L6
OUTPUT
26
25
21
22
11
PMOS
NMOS
12
7
27
28
27
28
15
17
19
65
INPUT
L6

FIG. 26

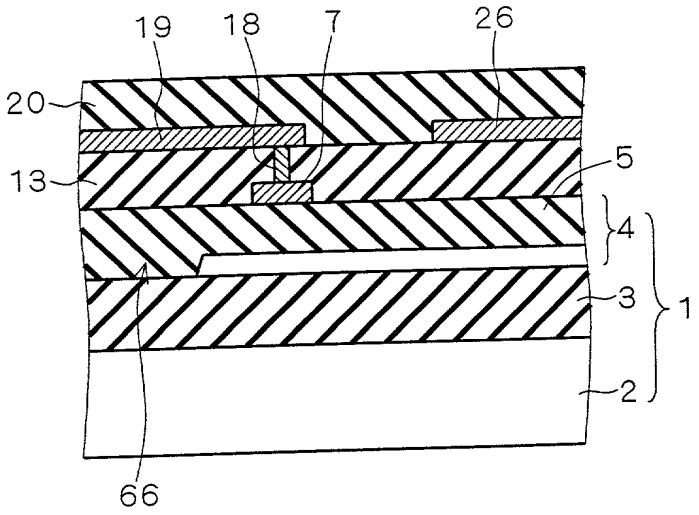
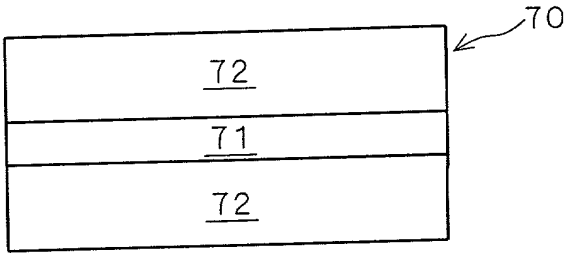


FIG. 27 (A)



LOGIC INVERSION

FIG. 27 (B)

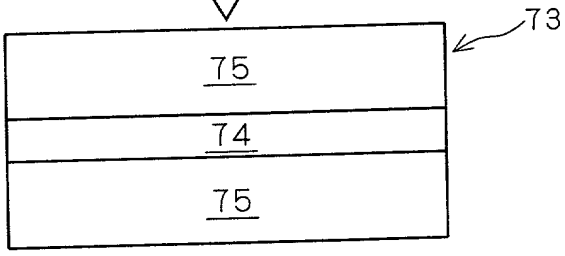


FIG. 28

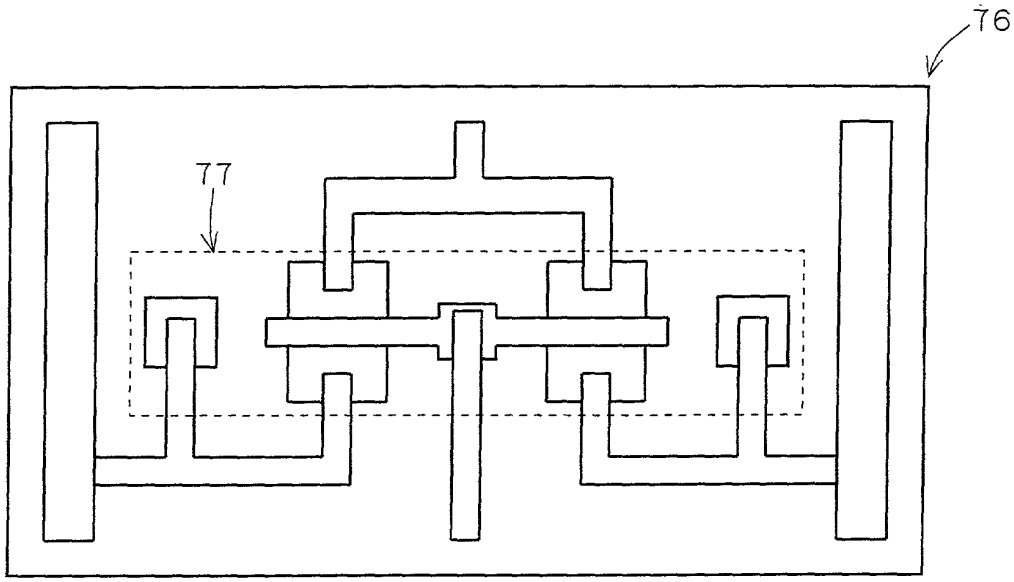


FIG. 29

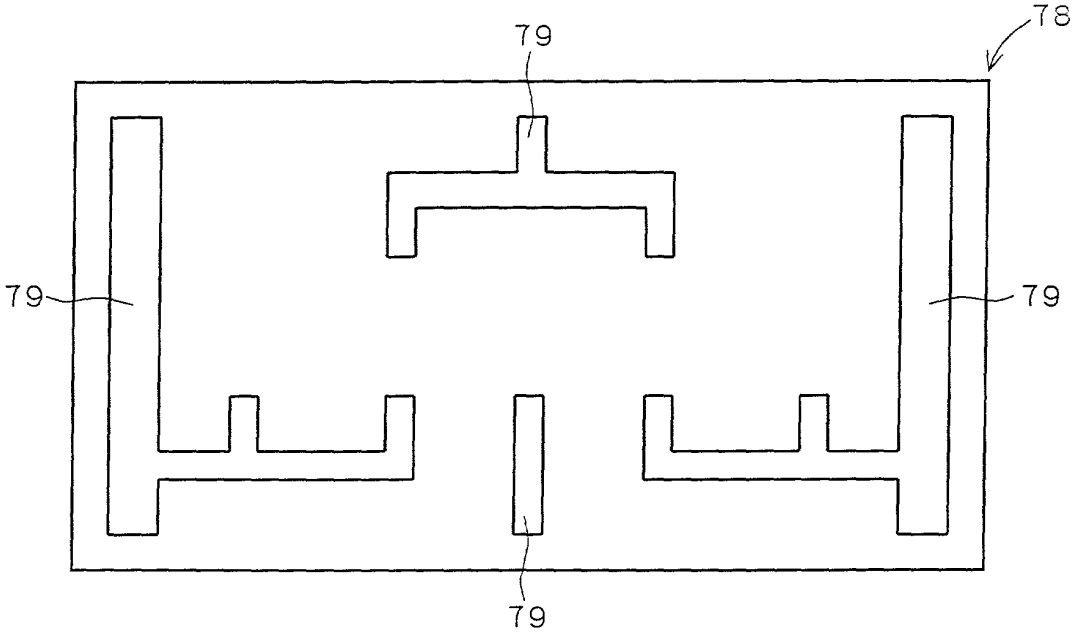


FIG. 30 (A)

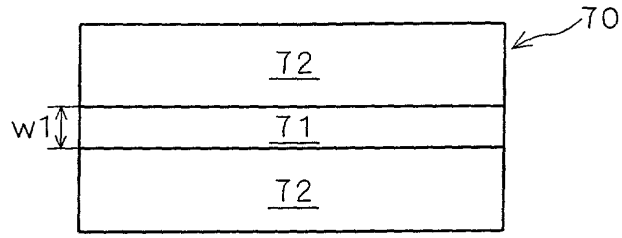


FIG. 30 (B)

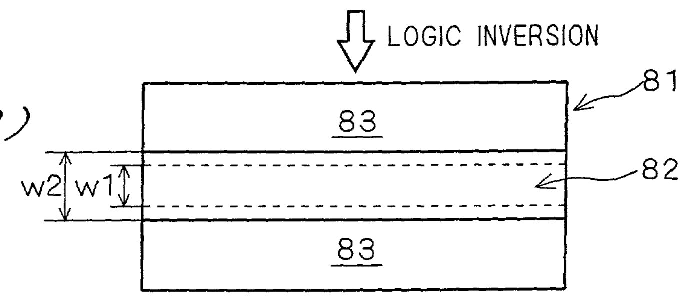


FIG. 30 (C)

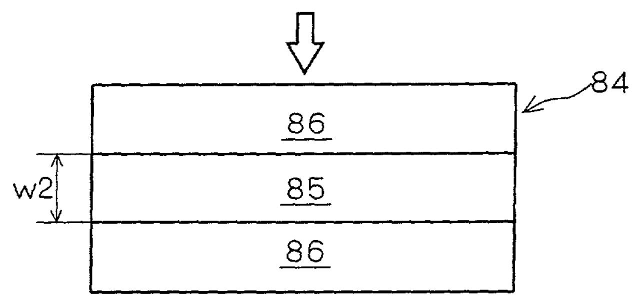


FIG. 31

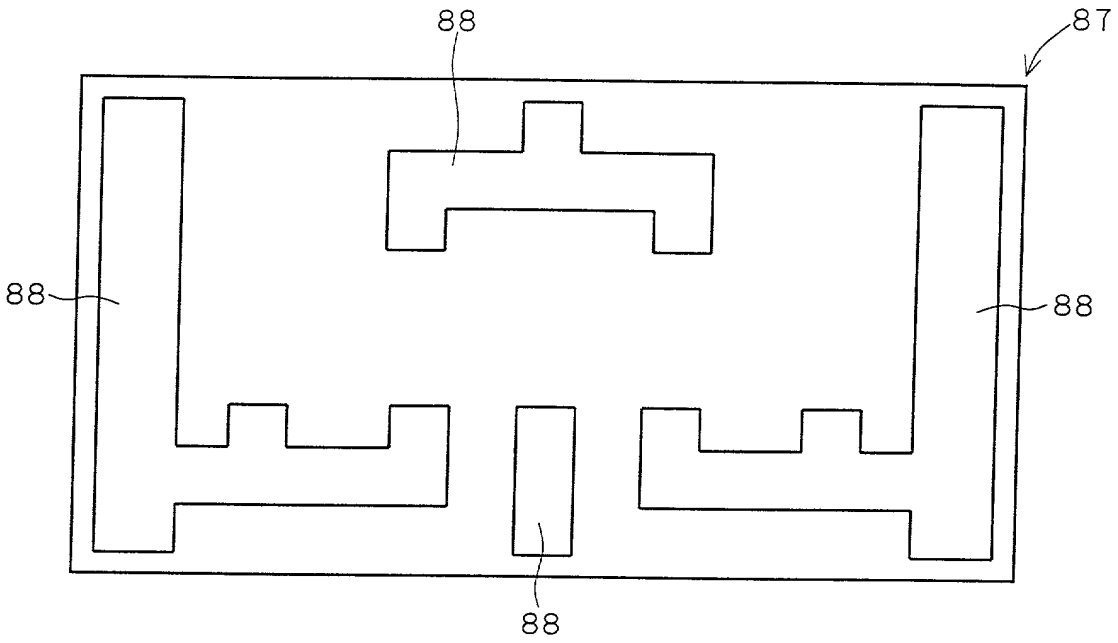


FIG. 32

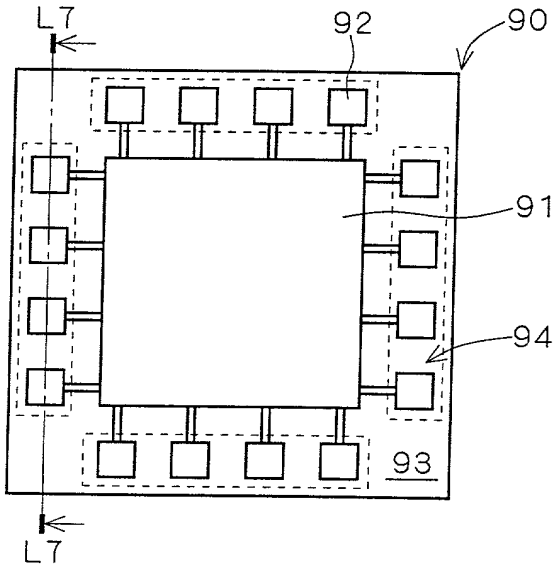


FIG. 33

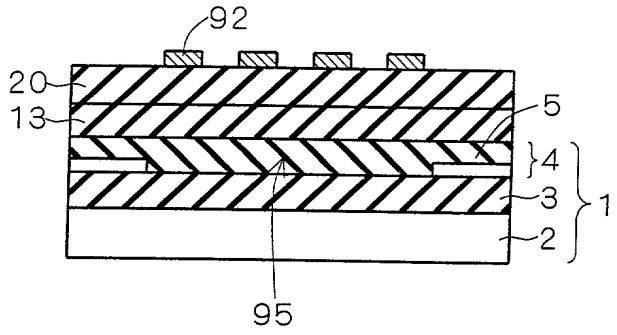

92
20
13
5
4
3
2
1
95

FIG. 34

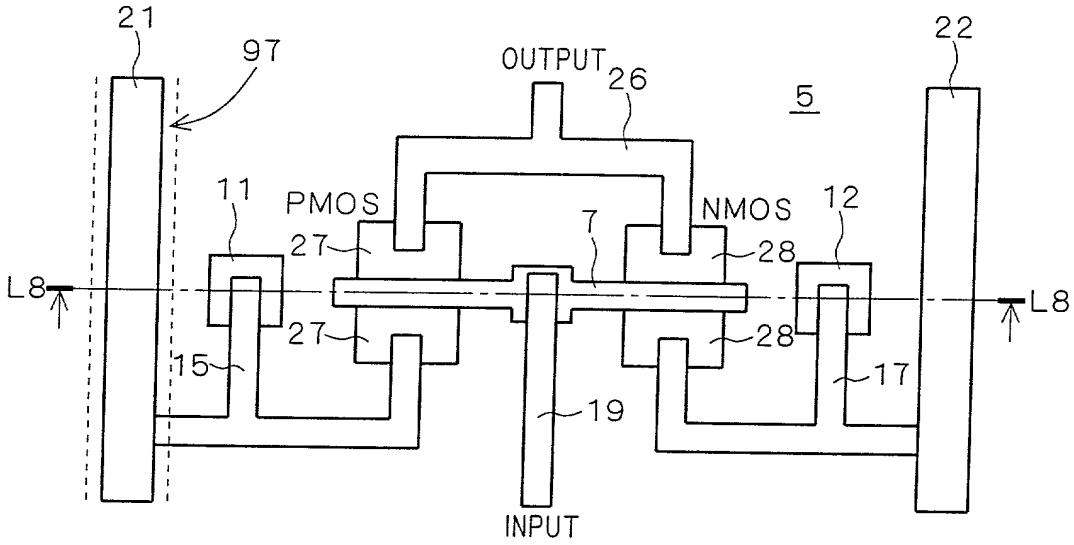
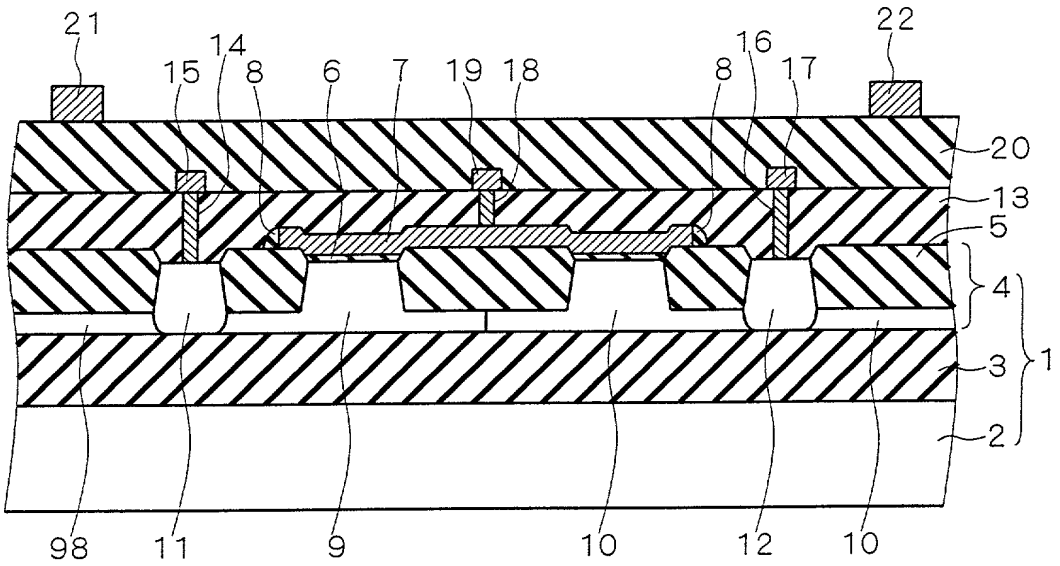

21
97
OUTPUT
26
5
22
11
PMOS
7
NMOS
12
27
28
L8
L8
27
28
15
17
19
INPUT

FIG. 35


21
14
15
8
6
7
19
18
8
16
17
22
20
13
5
4
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1
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98
11
9
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12
10

FIG. 36

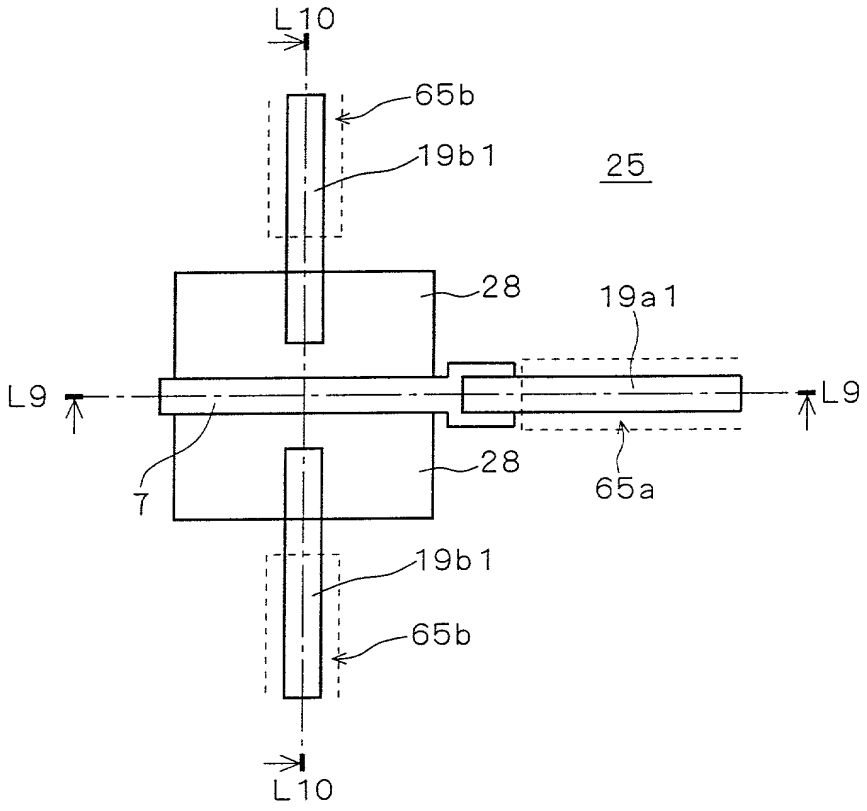
L10
65b
19b1
25
28
19a1
L9
L9
7
28
65a
19b1
65b
L10

FIG. 37

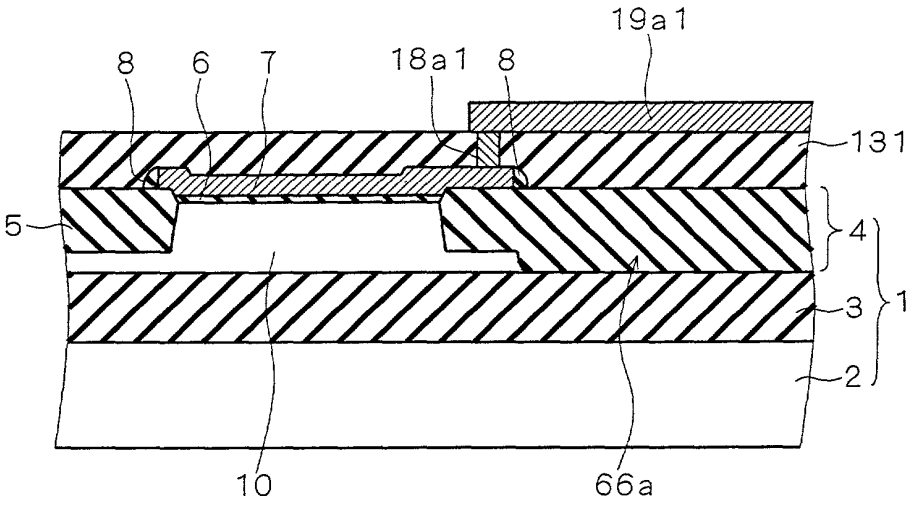
19a1
8
6
7
18a1
8
131
5
4
3
1
2
10
66a

FIG. 38

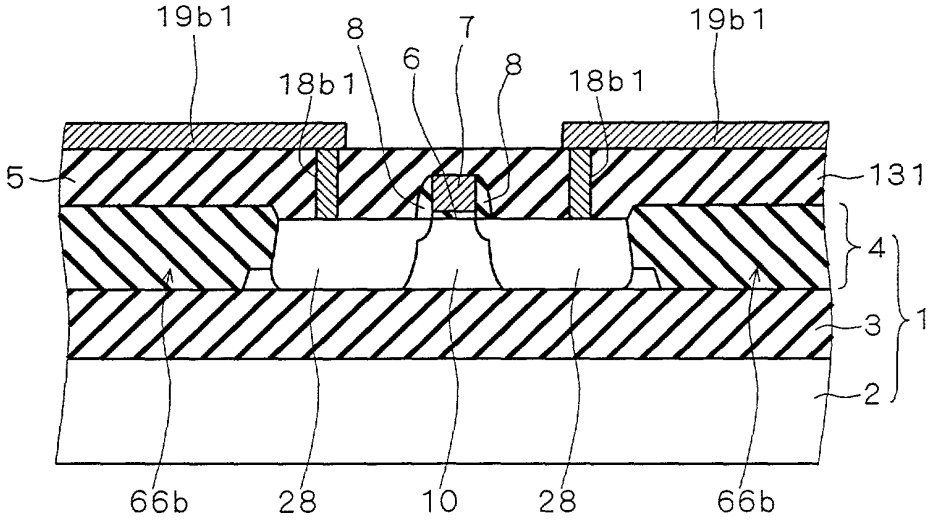
19b1
8
7
19b1
6
8
18b1
18b1
5
131
4
3
1
2
66b
28
10
28
66b

FIG. 39

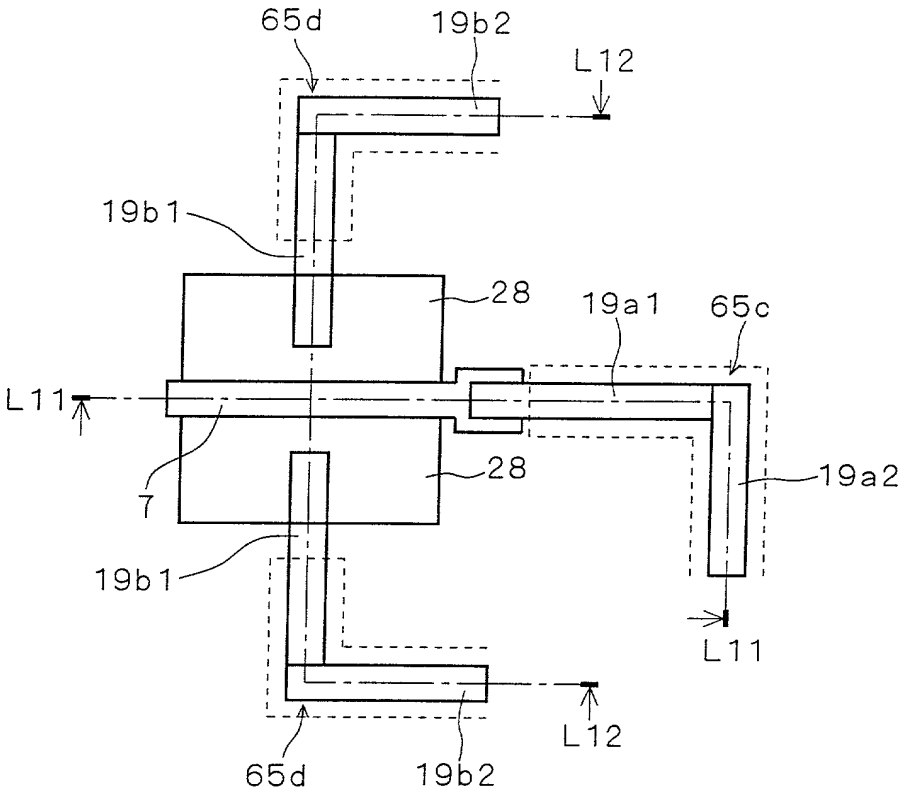
65d
19b2
L12
19b1
28
19a1
65c
L11
7
28
19a2
19b1
L11
L12
65d
19b2

FIG. 40

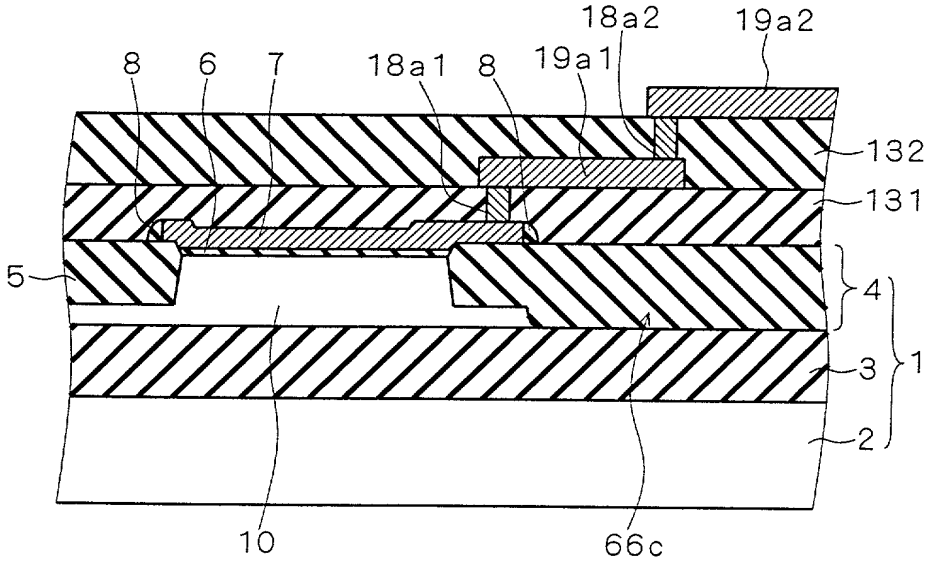
18a2
19a2
8
6
7
18a1
8
19a1
132
131
5
4
3
1
2
10
66c

FIG. 41

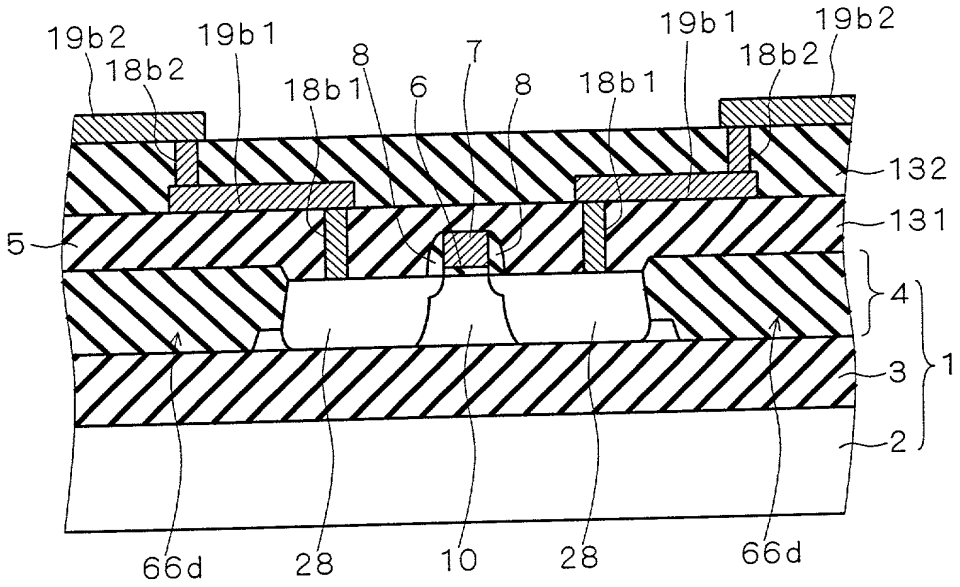
19b2
19b1
18b2
8
18b1
6
7
8
18b1
19b1
18b2
19b2
132
131
5
4
3
1
2
66d
28
10
28
66d

FIG. 42

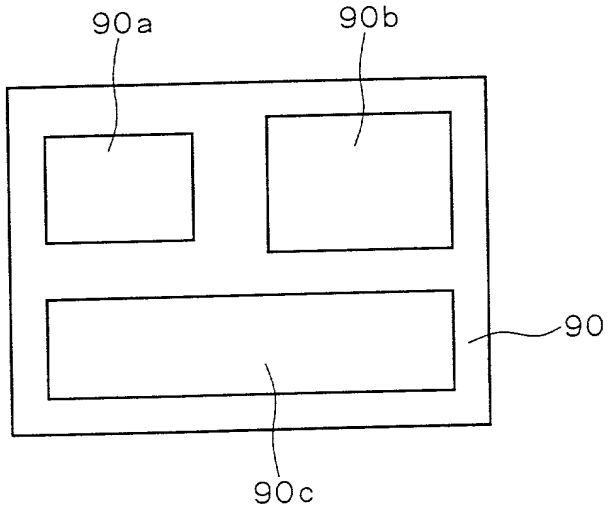
90a
90b
90
90c

FIG. 43

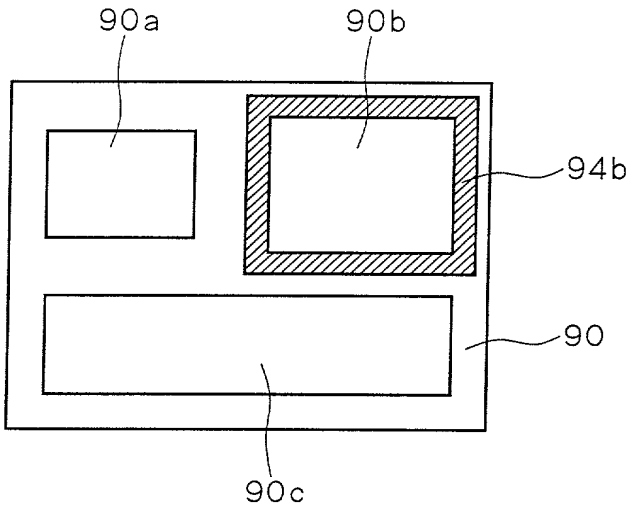
90a
90b
94b
90
90c

FIG. 44

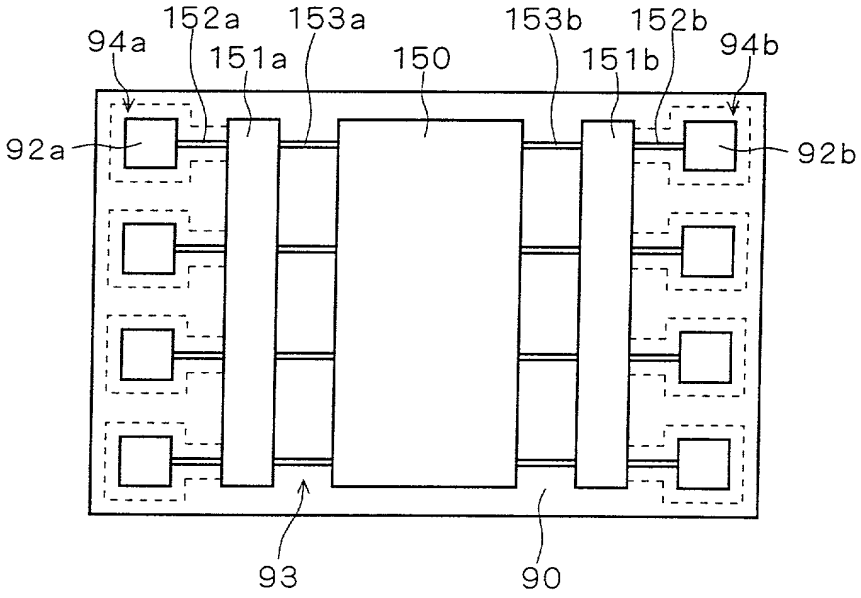
152a
153a
153b
152b
94a
151a
150
151b
94b
92a
92b
93
90

FIG. 45

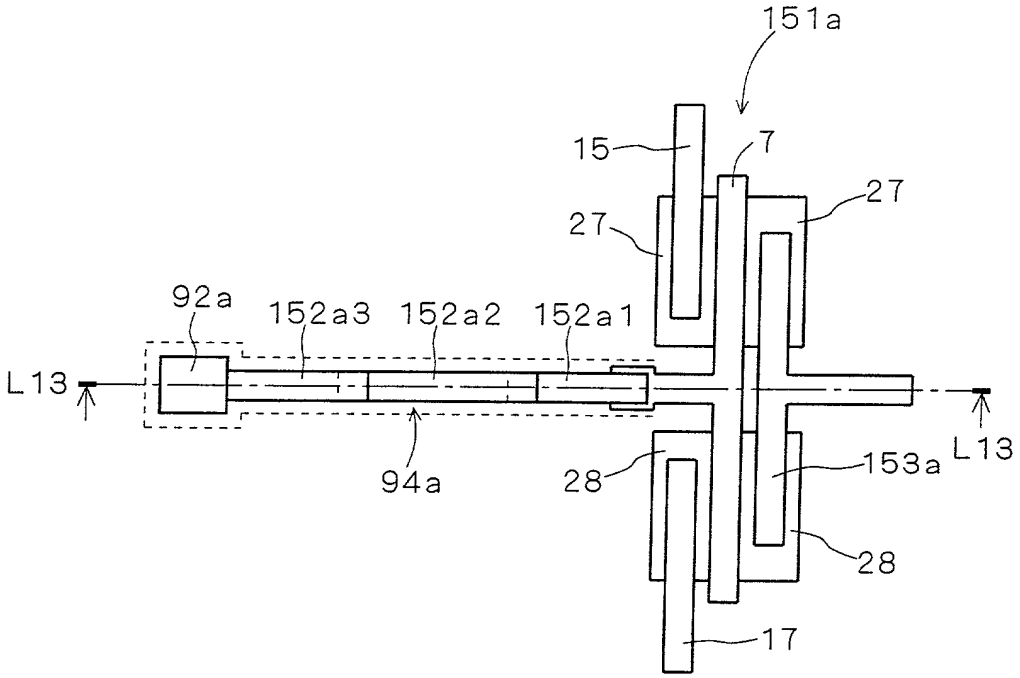
151a
15
7
27
27
92a
152a3
152a2
152a1
L13
94a
28
153a
L13
28
17

FIG. 46

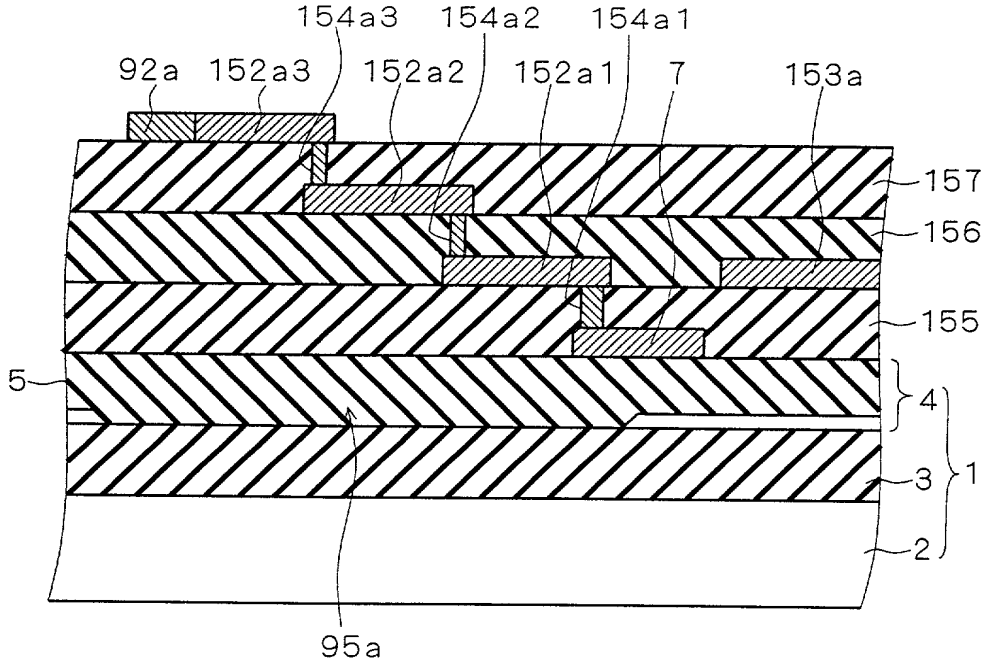
154a3
154a2
154a1
92a
152a3
152a2
152a1
7
153a
157
156
155
5
4
3
1
2
95a

FIG. 47

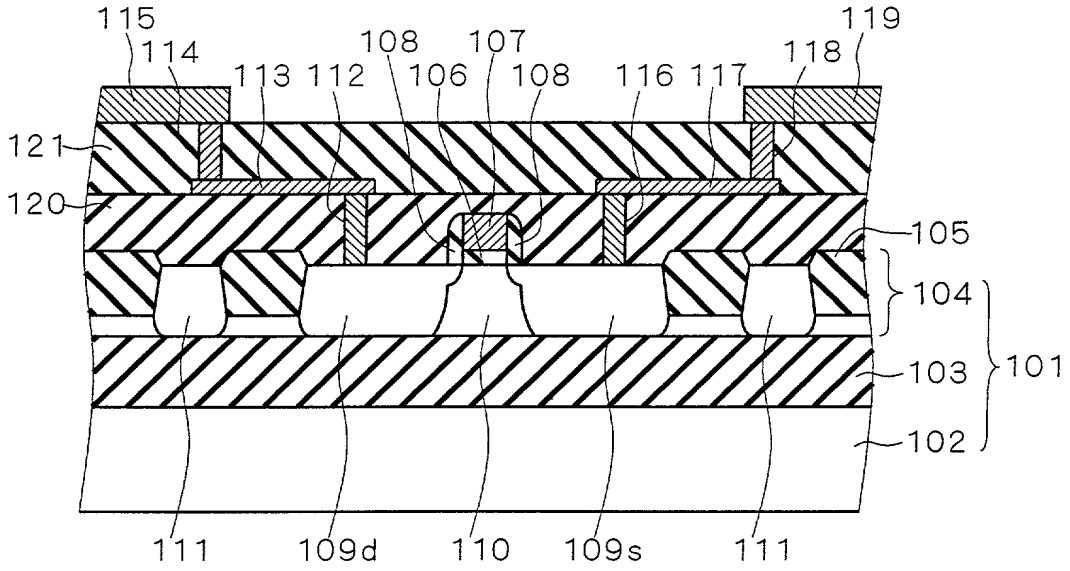
115
114
113
112
108
106
107
108
116
117
118
119
121
120
105
104
103
101
102
111
109d
110
109s
111

FIG. 48

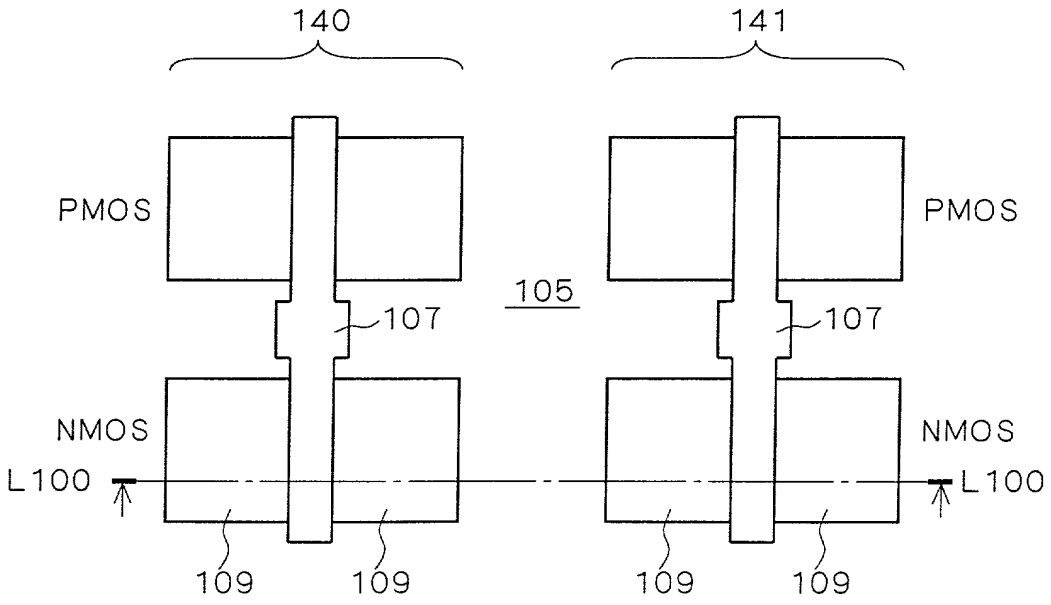
140
141
PMOS
PMOS
105
107
107
NMOS
NMOS
L100
L100
109
109
109
109

FIG. 49

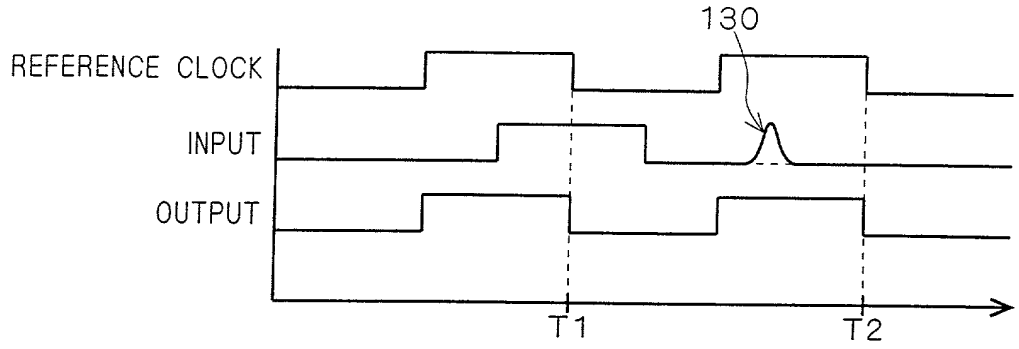

FIG. 50

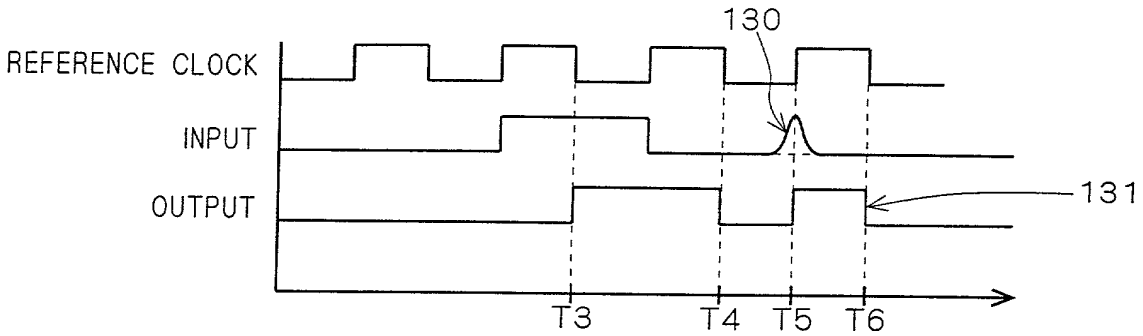

FIG. 51